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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,589	03/19/2004	Michael A. Kost	D2A1270-1	9254

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EXAMINER	
WANG, TED M	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
12/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/805,589	KOST ET AL.	
	Examiner	Art Unit	
	Ted M. Wang	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-8,10,11,13,15,16,18,19 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13,15,16,21* is/are allowed.

6)☒ Claim(s) *4,7,10 and 18* is/are rejected.

7)☒ Claim(s) *5,6,8,11 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The indicated allowability of claims 4-8, 10, 11, 13, 15, 16, 18, 19, and 21 are withdrawn in view of the newly discovered reference(s) to US 5,602,878 and US 6,970,435. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4, 10 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cross (US 5,602,878).

- With regard claim 1, Cross discloses a system comprising:

  a first set of storage locations (Fig.3 element 301);

  a second set of storage locations (Fig.3 element 305); and

  control logic (Fing.3 elements 302, 306, 303 and 304 configured to load data from a plurality of parallel data streams (Fig.3 element data bus 308 and column 5 lines 65-67) received according to a first clock signal having a first rate into the first set of storage locations (Fig.3 element 320), allow values of

the data to stabilize in the first set of storage locations (Fig.3 element 303, LSV (last stable value) and column 5 lines 1-11 and column 7 lines 1-19);

load data from the first set of storage locations to the second set of storage locations (Fig.3 element 308 and 301 and column 6 lines 1-8);

read data from the second set of storage locations according to a second clock signal (Fig.2 element 322) having a rate that is different from the rate of the first clock signal (column 5 lines 16-20);

determine a delay between data being loaded into the first set of storage locations and the same data being loaded into the second set of storage locations (column 7 lines 1-51);

and selectively add or drop data to maintain the delay in a predetermined range, and

delay logic configured to delay a load signal associated with the first set of storage locations (Fig.3 element 303, where the element 303 is considered as the delay logic) and to provide the delayed load signal (Fig.3 element 313).

Cross discloses all of the subject matter as described in the above paragraph except for specifically teaching control logic including a state machine and delayed load signal is provided to the state machine.

However, Cross teaches source clock control (Fig.1 element 105) comprising finite state machine and the destination clock control (Fig.1 element 106) also comprising a finite state machine (column 2 line 65 –

column 3 line 5). Examiner considers this limitation as an obvious system design choice for the improved circuitry of the data transfer technique (Fig.3).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have the control logic (Fig.3 elements 303, 304) to comprise a state machine as taught by Cross. Applicant has not disclosed that the state machine provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with the discrete device 303 304 because the control circuit 303 and 304 performs the same function as that of the state machine as recited in claim 1. Therefore, it wou"d have been obvious to one of ordinary skill in this art to modify Cross's control circuit 303, 304 to obtain the invention as specified in claim 1.

- With regard claim 10, Cross further discloses wherein the second clock rate is n times the first clock rate (column 5 lines 16-20, where since the second clock is different from the first clock, it is inherent that the second clock rate is n times the first clock rate.)
- With regard claim 18, which is a method claim related to claim 10, all limitation is contained in claim 10. The explanation of all the limitation is already addressed in the above paragraph.

4. Claims 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cross (US 5,602,878) in view of Buchanan et al. (US 6,970,435).

- With regard claim 7, Cross discloses all of the subject matter as described in the above paragraph except for specifically teaching a first set of storage locations, wherein the first set of storage locations comprises four storage locations and wherein each storage location is configured to store a bit from each of parallel data streams.

  However, Buchanan et al. teaches a first set of storage locations (Fig.2 element latch L1-L4), wherein the first set of storage locations (Fig.2 element latch L1-L4), comprises four storage locations and wherein each storage location is configured to store a bit from each of parallel data streams (Fig.2 element latch L1-L4 with data D0-D3, respectively).

  It is desirable to have the first set of storage locations comprises four storage locations and wherein each storage location is configured to store a bit from each of parallel data streams. The reason for that is that the interconnection system of the present invention is termed Data Aligned Serial Link (DASL) Interface and the DASL Interface receives data from a parallel interface such as a CMOS ASIC, partitions the bits from the parallel interface into a smaller number of parallel bit streams. The smaller number of parallel bit streams are then converted into a high speed serial stream, which is transported via a transmission medium to the receiver of the other module, so that the high speed data transferring can be reached to improve the communication speed.

Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include first storage location as taught by Buchanan et al. into Cross's source clock domain 302 to replace the Source Register 301 so as to improve the speed of the data transfer.

Allowable Subject Matter

5. Claims 13, 15, 16 and 21 allowed.

6. Claims 5, 6, 8, 11 and 19 are objected to as being dependent upon an objected claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2611

Ted M. Wang